09/816,967

1. (Currently Amended) A core for providing communications between a transmission media and a processor in a parallel serial architecture, said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages different numbers of said serial lanes to alter a speed of data passing through said core.

2. (Original) The core in claim 1, further comprising a data controller for controlling an operation of said selector.

3. (Currently Amended) The core in claim 1, wherein each of said serial lanes includes a buffer ~~buffers for performing additional speed alteration of said data~~.

4. (Original) The core in claim 3, wherein said buffers comprise elastic first in, first out (FIFO) buffers.

5. (Previously Presented) The core in claim 1, wherein said selector comprises a multiplexer.

6. (Original) The core in claim 1, wherein additional speed adjustment is attained by said selector engaging additional lanes.

7. (Original) The core in claim 1, wherein said transmission media operates at a different data speed than said processor.

8. (Currently Amended) A parallel-serial communication system comprising:

at least one processor;

at least one transmission media connecting said at least one processor; and

a core between each processor and said transmission media, said core providing communications between said transmission media and said processor, and said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages different numbers of said serial lanes to alter a speed of data passing through said core.

9. (Original) The parallel-serial communication system in claim 8, further comprising a data controller for controlling an operation of said selector.

10. (Currently Amended) The parallel-serial communication system in claim 8, wherein each of said serial lanes includes a buffer ~~buffers for performing additional speed alteration of said data.~~

11. (Original) The parallel-serial communication system in claim 10, wherein said buffers comprise elastic first in, first out (FIFO) buffers.

12. (Previously Presented) The parallel-serial communication system in claim 8, wherein said selector comprises a multiplexer.

13. (Original) The parallel-serial communication system in claim 8, wherein additional speed adjustment is attained by said selector engaging additional lanes.

14. (Original) The parallel-serial communication system in claim 8, wherein said transmission media operates at a different data speed than said processor.

15. (Currently Amended) A core for providing communications between a transmission media and a processor in a byte stripped parallel serial InfiniBand architecture, said core comprising:

serial lanes connecting said processor to said transmission media; and

at least one selector connected to said serial lanes, whereby said selector selectively engages different numbers of said serial lanes to alter a speed of data passing through said core.

16. (Original) The core in claim 15, further comprising a data controller for controlling an operation of said selector.

17. (Currently Amended) The core in claim 15, wherein each of said serial lanes includes a buffer ~~buffers for performing additional speed alteration of said data~~.

18. (Original) The core in claim 17, wherein said buffers comprise elastic first in, first out (FIFO) buffers.

19. (Previously Presented) The core in claim 15, wherein said selector comprises a multiplexer.

20. (Original) The core in claim 15, wherein additional speed adjustment is attained by said selector engaging additional lanes.

21. (Original) The core in claim 15, wherein said transmission media operates at a different data speed than said processor.